Amendments to the Specification:

Please replace the paragraph beginning on page 3, line 10 with the following amended paragraph:

An integrated semiconductor memory can be operated with a higher current for writing in and/or reading out information and which can be less susceptible to leakage currents. Generally, an integrated semiconductor including a web or ridge arranged on an insulation layer, a first source/drain region arranged on the insulation layer at one lateral end of the web, and a second source/drain region is arranged on the insulation layer at another lateral end of the web. Also, the two longitudinal sides of the web and a top side of the web can be covered with a layer sequence comprising a gate dielectric and a gate electrode.

Please replace the paragraph beginning on page 5, line 13 with the following amended paragraph:

The top side of the surface contact can be arranged below the level of the top side of the web and cab be electrically insulated from a word line passing the storage capacitor by an insulating upper filling structure. This word line (passing word line) can be formed at the same level as the word line, which can be connected to the selection transistor and can cover the top

side of the web. The passing word line running at the same level can be insulated from the top side of the upwardly shortened or recessed surface contact by the upper filling structure.

Please replace the paragraph beginning on page 7, line 21 with the following amended paragraph:

FIG. 1 shows an integrated semiconductor memory 10 with an SOI substrate 20. The buried insulation layer 11 can be arranged directly below the selection transistors 3 of the memory cells 1. The selection transistors can be formed at webs or ridges 4. The buried insulation layer, preferably oxide layer 11, can have openings in which a trench capacitor 2 can be incorporated into the substrate 20 and can be connected to a first source/drain region 5 of the selection transistor 3 by a contact arranged in the opening, a surface contact 19. The first source/drain region 5 can be situated at a first end A of the web 4 running in the longitudinal direction x, and the second source/drain region 6 can be arranged at the other lateral end B of the web. The web can extend between the ends A, B with its main extending direction x, which can coincide with the current flow direction I of the transistor channel, and can be surrounded from above and also on its side walls above and below the plane of the drawing by a gate oxide 9 and a gate layer sequence 16.

Please replace the paragraph beginning on page 9, line 15 with the following amended paragraph:

The storage capacitor 2 can have as outer capacitor electrode, either an electrode (buried plate) which can be arranged below the buried insulation layer 11 and can be arranged in the bulk material, or can include the doped, for example, heavily n-doped, substrate material of the semiconductor substrate 20. The inner capacitor electrode 12 can be isolated from the substrate 20 by a capacitor dielectric 13, which may ~~also~~ be a layer stack or layer sequence, in a topmost region below the insulation layer 11, where a collar region can be provided. The electrical connection between the inner capacitor electrode 12 and the first source/drain region 5 of the selection transistor 3 is produced by a surface contact 19.

Please replace the paragraph beginning on page 10, line 4 with the following amended paragraph:

FIG. 3 shows, in plan view, an arrangement of seven storage capacitors 2, which are connected toward the right-hand side to a respective selection transistor 3 formed in each case at a web 4. The storage capacitors 2 can be arranged below the buried insulation layer 11, whereas the selection transistors 3 can be arranged above the buried insulation layer 11. The word lines 16 can cross the longitudinal direction x of the webs 4 and can cover both longitudinal sides and the top side of the webs. As a result, a large channel width can be obtained. By using narrow webs which may be configured narrower in direction y, with the aid of spacers, than the distance between the bit lines 17, charge carriers in the semiconductor material of the web can be